DELAY-LOCKED LOOP (DLL) INTEGRATED CIRCUITS HAVING HIGH BANDWIDTH AND RELIABLE LOCKING CHARACTERISTICS

Abstract of the Disclosure

Delay-locked loops have high bandwidth locking characteristics that are less susceptible process, voltage and temperature (PVT) variations. These DLLs are configured to support transition from a partial feedback loop lock condition to a full feedback loop lock condition during a start-up time interval, in order to insure that a multi-cycle lock condition is established at the time the DLL's clock signal output becomes available. The DLL may include a variable delay line that is responsive to a reference clock signal, an auxiliary phase detector that is electrically coupled to the variable delay line, and a main phase detector that is responsive to the reference clock signal and a feedback clock signal (DLLCLK). The auxiliary phase detector may be an edge-triggered SR-type phase detector and the main phase detector may be a three-state phase frequency detector.

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